CLAIMS

1. A method of fabricating a mold for protective caps which will be applied to a wafer, the method comprising the steps of:
fabricating a first and a second cooperating mold halves from a semiconductor material using lithography;
the first half and second halves, when brought together defining an array of mold cavities for an array of wafer scale protective caps.

2. The method of claim 1, wherein:
at least one half includes ejection holes; the method further comprising the provision of an eject wafer having pins; and
locating the ejection wafer behind the half so that the pins enter the holes.

3. The method of claim 1, wherein:
the caps are intended for attachment to a wafer; and
the mold is fabricated from the same material as the wafer.

4. The method of claim 3, wherein:
the material is silicon.

5. The method of claim 1, wherein:
the array has a spacing which corresponds to a spacing of the wafer.

6. The method of claim 1, wherein:
the mold cavities are formed using cryogenic deep silicon etching techniques.

7. The method of claim 1, wherein:
the first half of the mold has a lower surface in which recesses are formed;
the second mold half having an upper surface in which grooves are formed;
the recesses and grooves defining the mold cavities.

8. The method of claim 1, wherein:
the first half has formed in it first eject holes;
there being provided a first half release wafer from which projects a number of pins;
locating the pins in registry with the first holes;
the first half having a thickness in the area of the first holes, the pins being longer than the thickness;
the first half release wafer having a first position in which the pins are flush with an interior end of the first holes; and
providing a gap between the first half and the first half release wafer when the first half release wafer is in the first position.

9. The method of claim 1, wherein:
the second half includes second eject holes formed through it;
there being provided a second half release wafer from which project pins;
locating the pins in registry with the second eject holes;
the second half having a thickness in the area of the second eject holes, the pins being longer than the thickness;
the second half release wafer having a first position in which the pins are flush with an interior end of the second eject holes;
there being a second gap between the second half and the second half release wafer when the second half release wafer is in the first position.

10. The method of claim 8, wherein:
the holes are formed by electron beam or X-ray lithography.

11. The method of claim 1, wherein:
the first and second halves are comprised of a semiconductor that is transparent to infrared light of a wavelength of about 1000 -5000 nm.

12. The method of claim 8, wherein:
the first and second halves and the first half release wafer are comprised of a semiconductor that is transparent to infrared light of a wavelength of about 1000 - 5000 nm.

13. The method of claim 8, wherein:
the pins are formed by electron beam or X-ray lithography.

14. The method of claim 1, wherein the first half includes first holes formed through it, and further comprising the steps of:
providing a first half release wafer from which project pins;
locating the pins in alignment with the first holes;
the first half having a thickness in the area of the first holes, the pins being formed longer than the thickness;
the first half release wafer having a first position in which the pins are flush with an interior end of the first holes;
locating a gap between the first half and the first half release wafer when the first half release wafer is in the first position;
forming second holes through the second half;
providing a second half release wafer from which projects pins;
locating the pins in alignment with the second holes;
the second half having a thickness in the area of the second holes, the pins being formed longer than the thickness;
the second half release wafer having a first position in which the pins are flush with an interior end of the second holes;
locating a second gap between the second half and the second half release wafer when the second half release wafer is in the first position.

15. The method of claim 14, wherein:
the pins and holes are formed by electron beam or X-ray lithography.

16. The method of claim 14, wherein:
the first and second halves and the first and second half release wafers are comprised of a semiconductor that is transparent to infrared light of a wavelength of about 1000 -5000 nm.

17. The method of claim 1, wherein:
locating in the first half, portions which separate adjacent areas;
locating in the second half, cooperating portions which separate adjacent mold features;
the portions and cooperating portions coming together when the halves are brought together such that material is squeezed out from between the first and second portions, separating adjacent caps.

18. The method of claim 1, wherein:
locating in the first half, portions which separate adjacent areas;
locating in the second half, cooperating portions which separate adjacent mold features;
the portions and cooperating portions coming together when the halves are brought together such that material is left as a thin layer between the first and second portions, the caps thus being intended, initially, as an array joined by the thin layer.

19. The method of claim 17, wherein:
the portions and cooperating portions are formed by electron beam or X-ray lithography.

20. The method of claim 17, wherein:
the portions and cooperating portions have un-etched top surfaces.